REMARKS

Claims 3 and 5-7 remain in the application. Claims 8-13 have been newly added.

The Office Action indicated that the subject matter of claim 5 would be allowable if rewritten in independent form (Office Action, Page 8 Lines 9-13). The indicated allowable subject matter of claim 5 has been incorporated into claims 6 and 7 to render those claims allowable also.

Applicant's invention, a layout check system, determines whether a bypass capacitor in a printed circuit board topology will be effective in protecting an integrated circuit (IC) from parasitic noise and high frequency power fluctuations. Design engineers frequently wire bypass capacitors in parallel with IC power pins to short high frequency signals to ground and supplement the power line charge during a switching transient. To be effective, however, the impedance between the power source and the bypass capacitor must be larger than the impedance between the power source and the IC power pin. Applicant's invention addresses this design concern by describing an apparatus and method that automatically determines in a CAD system the relative impedances and whether a bypass capacitor in a circuit layout will be effective pursuant to a novel algorithm.

Claim 3 was rejected under 35 U.S.C. 102 (e) as being unpatentable over *Sasaki* et al (US Pat No. 6,546,528), hereinafter *Sasaki* I. Applicant respectfully traverses.

It should be noted that the burden of establishing a *prima facie* case of obviousness lies with the Patent Office. *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988) (stating: "The PTO has the burden under section 103 to establish a *prima facie* case of obviousness"). To establish a *prima facie* case of obviousness, (1) there must be some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art)

to combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference must teach or suggest all the claim limitations. See *MPEP* §§ 2142-43.

Sasaki I describes a circuit board evaluation device that purports to determine if circuit resonance will occur, (*Sasaki* I, abstract). *Sasaki* asserts that printed circuit boards radiate unwanted electromagnetic waves, (*Sasaki*, Column 3, Lines 11-13). The object of Sasaki's invention is to minimize these unwanted electromagnetic waves by evaluating whether a printed circuit board is designed to avoid resonance, (*Sasaki* I, Column 4, Lines 45-49).

Claim 3 recites "wherein when a power via exists on wiring that connects the power pin and the bypass capacitor the calculation unit calculates, with use of the layout data, a shortest wiring distance between the power pin and the power via as the first value, and the shortest wiring distance between the power pin and the bypass capacitor as the second value". The Office Action asserts that this limitation is disclosed in *Sasaki I* (Office Action, Page 7, Lines 1-2). *Sasaki I* however fails to disclose or suggest making calculations when a power via exists between a power pin and a bypass capacitor.

Sasaki I discloses "The layout information data being extracted are made in connection with pads interconnected with power terminals and ground terminals of the active components installed in the signal layer 26a, lines and via holes for interconnecting the pads with the power source layer 28 or the ground layer 27 and decoupling capacitors 25a, 25b, 25c 25d as well as layout information data regarding the ground layer 27 and the power source layer 28, (*Sasaki*, Column 8 Lines 13, 20). *Sasaki I* fails to suggest that that the relative distance from a power via to a bypass capacitor and a power via to a power pin should be calculated. The lack of suggestion is further highlighted in the drawings where the decoupling capacitors 25 are

connected directly to the power terminal 23 with power applied to the power terminal 23 through a via from a power source layer 28, (*Sasaki I*, Figures 3a and 3b).

Sasaki I also explicitly teaches away from making the recited calculation by suggesting the use of an equivalent circuit that does not contain a power via between a power pin and a bypass capacitor.

> parasitic inductance and parasitic resistance of the pad and via hole being connected in series to the decoupling capacitor *25* are contained in an equivalent circuit of the decoupling capacitor, (*Sasaki I*, Column 9, Lines 35-40).

Calculations made using the *Sasaki I* equivalent are not directed to a circuit having a power via between the power pin and the bypass capacitor.

The recited calculation unit is important since the wiring distances determine the impedances from the power via to the power pin. If the impedance from the power via to the bypass capacitor is greater than the impedance from the power via to the power pin, the bypass capacitor will be ineffective at suppressing parasitic noise and power fluctuations. An ineffective bypass capacitor is a design defect that results in sporadic circuit board failures.

The Office Action also used a second *Sasaki* (U.S. Pat No. 6,297, 965) reference, hereinafter *Sasaki II*, to support a rejection of now canceled claim 4.

Sasaki II discloses a wiring arrangement for suppressing electromagnetic wave radiation emitted from a printed circuit board. *Sasaki II* asserts that by controlling line impedances unwanted electromagnetic radiation may be minimized, (*Sasaki II*, Abstract). *Sasaki II* suggests that line impedances be kept to less than 1/3 of the impedance at which electromagnetic radiation will occur. *Sasaki II* further suggests that keeping the impedances well below the resonance frequency helps to avoid unwanted electromagnetic radiation.

Sasaki II like *Sasaki I* fails to disclose or suggest the recited calculation unit for calculating the wiring distances recited in claim 3 as explained above, making claim 3 patentable over any combination of *Sasaki I and Sasaki* Applicant respectfully requests that the rejection be withdrawn.

Claims 8-12 have been added to recite an embodiment of the invention shown in figures 5 and 6. Claim 13 has been added to recite an embodiment of the invention shown in figures 5, 6 and 7. These claims present the same issues that are believed allowable from the above remarks.

In view of the submission of these amended claims, it is believed the case is now in condition for allowance and an early notification of the same is requested.

If the Examiner has any further suggestions with regards to this case, the undersigned attorney would appreciate any directions or comments.

I hereby certify that this correspondence is being transmitted via facsimile to the USPTO at 571-273-8300 on May 22, 2006.

By: Sharon Farnus

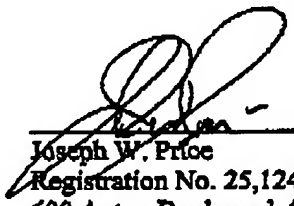
Sharon Farnus

Signature

Dated: May 22, 2006

Very truly yours,

SNELL & WILMER L.L.P.



Joseph W. Price
Registration No. 25,124
600 Anton Boulevard, Suite 1400
Costa Mesa, California 92626-7689
Telephone: (714) 427-7420
Facsimile: (714) 427-7799